Algorithmic Aspects of Problems Related to Optimization, Circuits, and Parameterized Complexity

Janio Carlos Nascimento Silva[1,2], **Uéverton dos Santos Souza**[1], **Luiz Satoru Ochi**[1]

[1]Instituto de Computação – Universidade Federal Fluminense (UFF)
Niterói – RJ – Brazil

[2]Instituto Federal do Tocantins (IFTO) – Campus Porto Nacional
Porto Nacional – TO – Brazil

janio.carlos@ifto.edu.br, {ueverton,satoru}@ic.uff.br

Abstract. *This thesis investigates several aspects of computational problems related to circuits and neighborhood exploration. Supported by a vast literature, we explore notable trends in algorithms, optimization, and computational complexity; and we provide some results for each topic discussed. The thesis' contributions are organized into four projects: (i) the study of* SUCCINCT MONOTONE CIRCUIT CERTIFICATION *(*SMCC*); (ii) the study of* BEST-CASE ENERGY COMPLEXITY IN SATISFYING ASSIGNMENTS *(*MINEC^+_M*); (iii) the proposition of the Th-hierarchy as an alternative to the hierarchy of complexity classes so-called W-hierarchy; and (iv) the study of the* MAXIMUM MULTI IMPROVEMENT *problem. Over the course of these four projects, we develop polynomial and parameterized reductions, NP-completeness proofs, classical and parameterized complexity analysis, and implementations of exact algorithms and metaheuristics.*

1. Introduction

In the last few decades, the resolution of hard combinatorial optimization problems has become one of the most prolific fields in Computer Science. Several studies address these problems from both theoretical and practical perspectives. In addition, the scientific community has dedicated efforts to understand the different levels of hardness and how problems behave in terms of tractability and structure. In this thesis, we present discoveries related to the computational complexity theory from three different perspectives:

- First, we address two measures in circuit complexity: The *certification-width* and the *energy complexity*. When dealing with monotone circuits, we prove the NP-Completeness of SUCCINCT MONOTONE CIRCUIT CERTIFICATION (SMCC) and BEST-CASE ENERGY COMPLEXITY IN SATISFYING ASSIGNMENTS (MINEC^+_M) even for planar circuits. We also prove that both problems are W[1]-hard, but SMCC belongs to W[P], while an XP-algorithm for MINEC^+_M is provided. After all, for both problems, we develop a pre-processing of input circuit (inspired by *win-win approach* strategies) where it was possible to prune graphs with bounded genus; this results in a structure whose treewidth is bounded. Hence, dynamic programming algorithms on tree decompositions were provided, solving the problems in FPT-time.
- In a second perspective, we present a hierarchy of classes of parameterized problems based on threshold circuit satisfiability – the *Th-hierarchy*. The study of

Th-hierarchy aims to understand possible gaps in the well-known W-hierarchy and the interaction Th-hierarchy *versus* W-hierarchy levelwise. We show that the hierarchies collapse in high levels (i.e., $W[P] = Th[P]$). Next, we study ways to convert threshold circuits into Boolean circuits with optimal depth; thus, we demonstrate that it is possible to construct an AKS sorting network in polynomial-time. This supports the prove that $Th[t] \subseteq W[SAT]$, for every $t \in \mathbb{N}$.

- Additionally, in an experimental front, we formalize the concept of neighborhood exploration called *Multi Improvement* (alternative to the traditional *First Improvement* and *Best Improvement*) and we build dynamic programming algorithms to solve the Maximum Multi Improvement Problem (MMIP) modeled as an inner step of a local search for TSP instances. Experiments have shown that this approach provides a possibility to perform fast neighborhood searches with high stability.

Note that all these approaches present novel concepts about problems in circuit complexity, computational complexity classes and neighborhood search. Because of this, we consider this thesis is a pioneer in circuit complexity studies and complexity classes in Brazil. All projects described in the Sections 2 to 5 have unprecedented formalization.

The full-text of the thesis are organized in four projects which are summarized in following sections. Some proofs and discussions were omitted in this document. Thus, we refer the full reading of [Silva 2021].

2. Succinct Certification

In the Chapter 2 of the thesis, we introduce the notion of *certification-width* of a monotone Boolean circuit, a complexity measure that intuitively quantifies the minimum number of edges that need to be traversed by a minimal set of positive weight inputs in order to certify that a given circuit is satisfied. We call the problem of computing this invariant as SUCCINCT MONOTONE CIRCUIT CERTIFICATION (SMCC). But first, consider the following definitions.

Definition 1. A Boolean circuit is a directed acyclic graph $C(V, E)$ having only one sink, where the set of vertices V is partitioned into $(I, G, \{v_{out}\})$: (i) a set of inputs $I = \{i_1, i_2, \dots\}$ composed of the vertices of in-degree 0; (ii) a set of gates $G = \{g_1, g_2, \dots\}$, which are vertices labeled with Boolean operators; (iii) and the single output (sink) vertex v_{out} with out-degree equal to 0 and also labeled with a Boolean operator. The input vertices represent Boolean variables that can take values from $\{0, 1\}$ ($\{\texttt{false}, \texttt{true}\}$), and the label/operator of a gate or output vertex w is given by $f(w)$.

In this chapter, we only deal with monotone circuits.

Definition 2. A monotone circuit is a Boolean circuit where the Boolean operators allowed are in $\{\texttt{AND}, \texttt{OR}\}$.

Definition 3. An *assignment* of a circuit C is a vector $X = [x_1, x_2, \dots, x_{|I|}]$ of values for the set of inputs I, where for each j, $x_j \in \{\texttt{false}, \texttt{true}\}$ is the value assigned to input i_j. We say that X is a satisfying assignment if C evaluates to `true` when given x as input.

Definition 4. Given a monotone circuit C with a satisfying assignment X, an edge (v_j, v_k) is considered critical to $X \to C$ if v_j evaluates to `true` and there is a path P from v_k to v_{out} in which all gates along P (including v_{out}) also evaluate to `true`.

Definition 5. Given a monotone circuit C, and a satisfying assignment X of C, a *positive certificate* for $X \rightarrow C$ is a connected subgraph of C formed by the critical edges and their respective vertices.

Since a positive certificate may have redundant edges, next, we present the notion of *succinct certificate*; and *certification-width* of C.

Definition 6. Given a monotone circuit C, and a satisfying assignment X of C, a *succinct certificate* for $X \rightarrow C$, is a connected subgraph $SC_{X \rightarrow C}$ of its positive certificate such that:

- v_{out} is a vertex of $SC_{X \rightarrow C}$; and
- for every vertex v of $SC_{X \rightarrow C}$ holds that
  - if $f(v) = \texttt{AND}$, then every in-edge of v is in $SC_{X \rightarrow C}$;
  - if $f(v) = \texttt{OR}$, then exactly one in-edge of v is in $SC_{X \rightarrow C}$.

The size of a succinct certificate $SC_{X \rightarrow C}$ is the number of edges of $SC_{X \rightarrow C}$.

Definition 7. The certification-width of a monotone circuit C is the minimum size among all possible succinct certificates on all satisfying assignments of C.

Now, we have all elements to describe our main problem.

SUCCINCT MONOTONE CIRCUIT CERTIFICATION (SMCC)
Instance: A monotone circuit C; a positive integer k.
Goal: Determine whether the certification-width of C is at most k.

We denote by k-SMCC the parameterized version of SUCCINCT MONOTONE CIRCUIT CERTIFICATION where k is the parameter.

As a first result, we prove that SMCC is NP-complete even when the input monotone circuit is planar.

Theorem 1. SMCC is NP-complete even restricted to planar circuits.

The proof is based on a reduction from PLANAR VERTEX COVER.

2.1. Parameterized complexity

Subsequently, we show that k-SMCC, the problem parameterized by the size of the solution, is W[1]-hard, but still in W[P]. In contrast, we show that k-SMCC is fixed-parameter tractable when restricted to monotone circuits of bounded genus.

Lemma 1. k-SMCC is in W[P].

The proof follows from a reduction to WEIGHTED CIRCUIT SATISFIABILITY.

Theorem 2. k-SMCC is W[1]-hard.

We prove the W[1]-hardness of k-SMCC using a reduction from MULTICOLORED CLIQUE, a well-known W[1]-complete problem.

Using Radius Theorem from [Robertson and Seymour 1984] we are able to either solve k-SMCC on planar circuits or output an equivalent instance C' with treewidth bounded by a function of k (as stated in Lemma 2).

Lemma 2. Let (C, k) be an instance of SMCC with $n = |V(C)|$ and $m = |E(C)|$. There is an algorithm that in $O(n + m)$ time either solves (C, k) or outputs an instance (C', k) of SMCC such that:

- (C', k) is an yes-instance of SMCC if and only if (C, k) is also an yes-instance;
- C' is an induced subcircuit of a circuit C^* that has diameter at most $2k$ and it is also an induced subcircuit of C.

The proof of Lemma 2 is based on a preprocessing algorithm which prunes the circuit C in order to produce C'.

Lemma 3. Let (C, k) be an instance of SMCC. There is an algorithm that in $O(n^2 + nm)$ time either solves (C, k) or outputs an instance (C', k) of SMCC having depth at most k, such that (C', k) is an yes-instance of SMCC if and only if (C, k) is also an yes-instance.

Now, a reasoning similar to [Robertson and Seymour 1984] can be used from [Kanj et al. 2017] where genus is the bounded property of a circuit.

Lemma 4. Let C' be the circuit obtained from Lemma 3. It holds that C' has treewidth at most $(4k + 10) \cdot (g + 1)^{3/2}$, where g is the genus of C'.

From Lemma 4, in order to solve k-SMCC on bounded genus graphs, it is enough to present an FPT algorithm parameterized by the treewidth of C.

Theorem 3. k-SMCC can be solved in time $2^{O(tw)} \cdot n$, where tw is the treewidth of C.

The proof of Lemma 3 is a dynamic programming on nice tree decompositions.

3. Energy Complexity

In the Chapter 3 of the thesis, we deal with a circuit complexity measure called *energy complexity* (EC). The idea behind this measure is to evaluate the number of gates in a circuit that returns `true` for an assignment. The neuroscience literature argues that the activation of neurons in a human brain happens sparsely. It was shown in [Lennie 2003] that the metabolic cost of a single spike in cortical computation is very high in a way that approximately 1% of the neurons can be activated simultaneously. This phenomenon happens due to the asymmetric energy cost between neurons activated and non-activated in natural cases. From the other side, digital circuits, when satisfied (outputting `true`), on average activate 50% of the gates. This dilemma *artificial vs natural* was discussed in [Uchizawa et al. 2006] triggering the first statement of the term *Energy Complexity*.

After a previous analysis, we realize that Energy Complexity and Certification-width are closely related. Meanwhile Certification-width concerns to activated edges, Energy Complexity is about activated vertices. Naturally, we focus in understand which conclusions of Chapter 2 can be transported to a computational problem based on Energy Complexity. We define such a problem as BEST-CASE ENERGY COMPLEXITY IN SATISFYING ASSIGNMENTS (MINEC^+_M).

Given a Boolean circuit C and an assignment X, the Energy Complexity of X into C, $EC(C, X)$, is defined as the number of gates that output `true` in C according to the assignment X. The (Worst-Case) Energy Complexity of C (denoted by $EC(C)$) is the maximum $EC(C, X)$ among all possible assignments X (See [Dinesh et al. 2020]). Analogously, the Best-Case Energy Complexity of C (denoted by $MinEC(C)$) is the minimum $EC(C, X)$ among all possible assignments X.

BEST-CASE ENERGY COMPLEXITY OF SATISFYING ASSIGNMENTS IN MONOTONE CIRCUITS – MINEC^+_M
Instance: A monotone Boolean circuit C and a positive integer k.
Question: Is there a satisfying assignment X for C such that $EC(C, X) \leq k$?

We denote by k-MINEC$_M^+$ the natural parameterized version of MINEC$_M^+$.

Using a reduction from PLANAR VERTEX COVER we are able to show that MINEC$_M^+$ is NP-complete even when restrict to planar circuits. Our NP-completeness proof follows from a reduction from similar to that employed in Chapter 2.

Theorem 4. MINEC$_M^+$ is NP-complete even when restricted to planar circuits.

Additionally, we state some results regarding Parameterized Complexity. Here, some conclusions from Chapter 2 can not be transferred to Chapter 3. In the full-text thesis, we detail all main differences between SMCC and MINEC$_M^+$. For MINEC$_M^+$, it is needed to verify the possibility of 'leak of a `true` signal' in a specific situation where a satisfied gate is in-neighbor of a not-satisfied `AND`-gate.

Theorem 5. k-MINEC$_M^+$ is in XP.

The proof of Theorem 5 is given by an XP-algorithm.

Theorem 6. k-MINEC$_M^+$ is W[1]-hard.

This hardness proof is also given by a reduction from MULTICOLORED CLIQUE.

The following statements also uses the reasoning based on Grid Minor Theorem and the lemma from [Kanj et al. 2017] about genus, and finally, after a clever dynamic programming (which proves Theorem 7) we can write an FPT-algorithm for k-MINEC$_M^+$.

Lemma 5. Let (C, k) be an instance of MINEC$_M^+$. There is an algorithm that in polynomial time either solves (C, k) or outputs an equivalent instance (C', k) of MINEC$_M^+$ where each vertex is at distance at most $2k + 1$ from v_{out} in the underlying graph of C'.

Corollary 1. MINEC$_M^+$ is fixed-parameter tractable when restricted to monotone circuits having bounded maximum in-degree.

Lemma 6. Let C' be the circuit obtained from Lemma 5. It holds that C' has treewidth at most $(8k + 14) \cdot (g + 1)^{3/2}$, where g is the genus of C'.

Theorem 7. MINEC$_M^+$ can be solved in time $2^{O(tw)} \cdot n$, where tw is the treewidth of C'.

4. Th-hierarchy

The third project developed in this thesis still address questions about circuits, but, here we use circuits as tools for Complexity Classes studies. We introduce the *Th-hierarchy*, a natural generalization of the W-hierarchy defined by unweighted *threshold* circuit satisfiability problems. Investigating the relationship between Th-hierarchy and W-hierarchy, we discuss the complexity of transforming Threshold circuits into Boolean circuits, and observe that sorting networks are powerful tools to handle such transformations. Before entering in the main topics of this summary, we hardly encourage the reading of [Silva 2021] and [Downey and Fellows 2012].

The characterization of decision problems as WCS(t, h) in standard Boolean circuits has widespread attention, especially considering the enormous advance in Parameterized Complexity Theory. When classifying a problem in the W-hierarchy, in short, we are encapsulating the parameterized intractability of this problem in terms of satisfiability of a corresponding circuit based on Boolean functions (`AND`, `OR` and `NOT`). Thus, some questions emerge. Is W-hierarchy comprehensive enough? Are there problems complete considering a more general basis of functions?

Due to these questions, our curiosity turns into the *threshold circuits*.

Next, we present some conventions and preliminaries that are important for the sequence of this section (See more preliminaries in Chapter 4 from [Silva 2021]).
Definition 8 (Decision threshold circuits)**.** A decision threshold circuit is a decision circuit containing `AND` gates, `OR` gates, `NOT` gates, and `unweighted threshold` gates, where an `unweighted threshold` gate computes an unweighted threshold function.

Our generalization of WCS(t, h) by considering threshold circuits is as follows.

WEIGHTED WEFT t DEPTH h THRESHOLD CIRCUIT SATISFIABILITY – WTCS(t, h)
Instance: A decision threshold circuit C with weft t and depth h.
Parameter: A positive integer k.
Question: Does C has a satisfying assignment of weight k?

Similarly, we present the complexity classes Th[t].
Definition 9. A parameterized problem Π belongs to the class Th[t] if and only if Π is fixed-parameter reducible to WTCS(t, h) for some constant h.

Analogously, we define WEIGHTED THRESHOLD CIRCUIT SATISFIABILITY (WTCS) and Th[P] as a generalization of WCS and W[P] by considering decision threshold circuits instead of decision Boolean circuits. In addition, we define the generalization of WSAT as follows.

WEIGHTED TREELIKE THRESHOLD CIRCUIT SATISFIABILITY – WTTSAT
Instance: A decision threshold circuit C whose graph induced by its gates is isomorphic to a tree (treelike circuit).
Parameter: A positive integer k.
Question: Does C has a satisfying assignment of weight k?

Thus, the *Th-hierarchy* is as follow: $Th[1] \subseteq Th[2] \subseteq \cdots \subseteq Th[SAT] \subseteq Th[P]$.

By definition, it holds that

W[t] $\subseteq$ Th[t] (for every $t \in \mathbb{N}$) as well as W[SAT] $\subseteq$ Th[SAT] and W[P] $\subseteq$ Th[P].

At this point, some questions emerge such as

"W[P] = Th[P]?", "W[SAT] = Th[SAT]?", and "W[1] = Th[1]?"

To understand the relationship between these classes (at the highest levels), we revisit the Sorting Network field and present a time complexity analysis for the construction of AKS sorting networks, see [Paterson 1990].

Although the W-hierarchy is a set of infinite classes of parameterized problems, it may possible that the W-hierarchy is not complete in the sense that may exist a parameterized problem Π such that $\Pi \in$ W[$t+1$]; $\Pi \notin$ W[t]; Π is hard for W[t]; but, Π is not complete for W[$t+1$], for some t. Then, it is possible that there are problems between W[t] and W[$t+1$], or between W[SAT] and W[P]. Therefore, one of the motivation of the work in this section is consider classes based on threshold circuits to identify potential gaps in the W-hierarchy.

By definition, the following lemma is clear.

Lemma 7. $W[t] \subseteq Th[t]$, for every $t \in \mathbb{N}$.

In contrast, it is not clear if $Th[t] \subseteq W[t]$ for some t. We begin our discussion by disregarding structural constraints, which leads us to the ***W[P] versus Th[P]*** dilemma.

To show that Th[P] $\subseteq$ W[P] it is enough to present a fixed-parameter reduction from WEIGHTED THRESHOLD CIRCUIT SATISFIABILITY to WEIGHTED CIRCUIT SATISFIABILITY. In this case, it suffices to provide a way to locally replace each unweighted threshold gate for an equivalent Boolean circuit. For that, we consider the *Sorting Networks*. Therefore, based on Lemma 8, the Theorem 8 holds.

Lemma 8. Given an unweighted threshold gate T with n inputs and threshold t, in polynomial time with respect to n, one can construct an decision Boolean circuit C_T (a sorting network) such that C_T computes the same function of T.

Theorem 8. It holds that $Th[P] = W[P]$.

To show the W[SAT]-membership of Th[t], for every $t \in \mathbb{N}$, we first ensure the existence of a polynomial-time algorithm that converts a threshold gate (with fan-in n) in Boolean circuit with $O(\log n)$ depth. We know that the AKS sorting networks have logarithmic depth, and by construction its gates has bounded fan-out. In addition, after a complexity analysis developed in the thesis, it was possible to state the Proposition 1.

Proposition 1. One can construct an AKS sorting network in polynomial time.

Therefore, we can replace each unweighted threshold gate for an equivalent decision Boolean circuit by first construct an AKS network and then converting it into a treelike sub-circuit. After that, to obtain a complete treelike circuit, it is enough to handle with the gates inter sorting networks, which can be done since instances of WCS(t, h) have depth bounded by h, which is a constant. Hence, in polynomial time one can take an instance of WTCS(t, h) and outputs an equivalent treelike Boolean circuit C, i.e., a decision circuit corresponding to a Boolean formula. Thus, WTCS(t, h) is fixed-parameter reducible to WSAT and Th[t] $\subseteq$ W[SAT], for each $t \in \mathbb{N}$.

Lemma 9. For each $t \in \mathbb{N}$, it holds that Th[t] $\subseteq$ W[SAT].

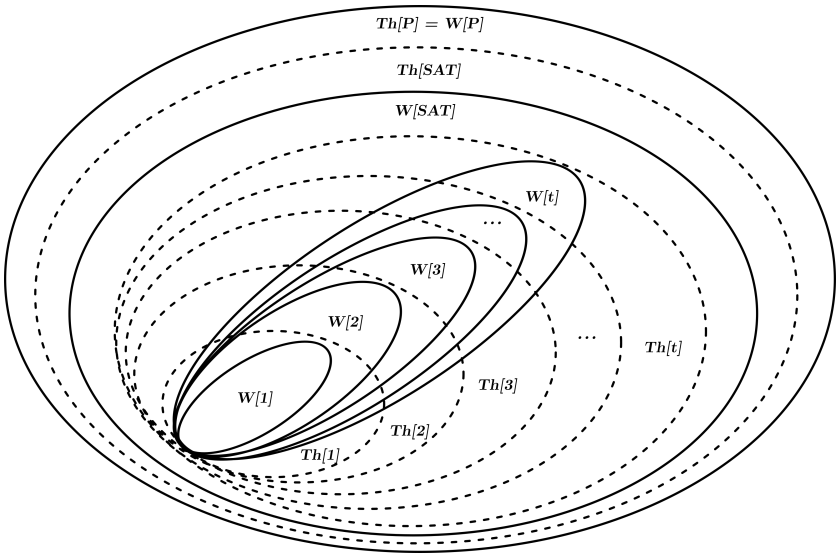

Figura 1. Relationship between W-hierarchy and Th-hierarchy.

Figure 1 shows the inclusion relationships we know between the W and Th classes.

5. Multi Improvement

Finally, the fourth project of this thesis have a different nature. Here, we analyze an interesting insight called Multi Improvement, which is a local search strategy based on neighborhood exploration for (meta)heuristics. In order to present a formal description for the MAXIMUM MULTI IMPROVEMENT PROBLEM (MMIP), we first present some theoretical background.

In Chapter 5 of the thesis, we consider the problem of finding a maximum set of independent moves from a given neighborhood structure, which is defined as the MAXIMUM MULTI IMPROVEMENT PROBLEM (MMIP).

MAXIMUM MULTI IMPROVEMENT PROBLEM
Instance: An instance I of an optimization problem Π; a feasible solution P of I; an evaluation function f according to Π; and a neighborhood operator ψ.
Goal: Determine a set S of independent moves according to ψ to be applied to P in order to obtain a feasible solution P' that maximizes $f(P')$.

In other words, MAXIMUM MULTI IMPROVEMENT PROBLEM consists of the following:

- An instance I of an optimization problem Π, an objective function f for Π, a feasible solution P of I, and a neighborhood operator ψ;
- Let $M = \{m_1, m_2, \dots m_\ell\}$ be the set of moves given by a neighborhood operator ψ, such that the neighborhood $\psi(P)$ of P is defined as

$$\psi(P) = \{P'_1 = m_1(P), P'_2 = m_2(P), \dots, P'_\ell = m_\ell(P)\};$$

- Let $g(m', P)$, a function that returns the gain/loss when $m' \in M$ is applied on P, i.e.

$$g(m', P) = f(m'(P)) - f(P).$$

- Let $\sigma(m_i, m_j)$, a function that returns 1 if $\{m_i, m_j\} \in M$ are independent of each other and returns 0, otherwise. This can be defined formally as

$$\sigma(m_i, m_j) = 1 \iff [g(m_i, P) = g(m_i, m_j(P))] \wedge [g(m_j, P) = g(m_j, m_i(P))];$$

- Consider also a decision variable $x_i \in \{0, 1\}$ that represents if a move $m_i \in M$ will be selected (1, case positive)

  The solution for the MMIP is a set of moves that maximizes Eq. (1).

$$maximize \sum_{i \in 1..|\psi(P)|} x_i \cdot g(m_i, P) \tag{1}$$

  Subject to:

$$x_i + x_j \leq 1, \text{ if } \sigma(m_i, m_j) = 0 \tag{2}$$

Theorem 9. MMIP $\propto$ WEIGTHED CLIQUE PROBLEM.

Theorem 9 is proved by a polynomial reduction from MMIP to WEIGTHED CLIQUE PROBLEM. This give us a notion of a difficult to solve MMIP by exact algortihms.

However, we developed three polynomial-time dynamic programming algorithms for solving the MMIP problem, when

$$\Pi = \text{TRAVELING SALESMAN PROBLEM},$$

and the neighborhood operator $\psi \in \{2\text{-Opt}, 3\text{-Opt and OrOpt-}k\}$

Several experiments are performed and the analysis suggest the rise of a new open topic focused on developing novel efficient neighborhood searches based on Multi Improvement. Experiments attested that, unlike FI and BI, MI has good stability, a fact that guarantees a estimation of the cost of the partial solution at a given step of the search.

6. By-products

The achievements of this thesis has appeared (until this moment) in the following international journals and conferences:

- *Maximum Multi Improvement on neighborhood exploration*
  Optimization Letters, v. 16, p. 97–115, 2022.
- *Succinct certification of monotone circuits.*
  Theoretical Computer Science, v. 889, p. 1-13, 2021.
- *Succinct Monotone Circuit Certification: Planarity & Parameterized Complexity.*
  COCOON - The 26th International Computing and Combinatorics Conference, LNCS 12273, p. 496–507, 2020.
- *Energy Complexity of Satisfying Assignments in Monotone Circuits: On the Complexity of Computing the Best Case.*
  AAIM - The 15th International Conference on Algorithmic Aspects in Information and Management, LNCS 13153, p. 380–391, 2021.
- *Parameterized Complexity Classes Defined by Threshold Circuits: Using Sorting Networks to Show Collapses with W-hierarchy Classes.*
  COCOA - The 15th Annual International Conference on Combinatorial Optimization and Applications, LNCS 13135, p. 348-363, 2021.

The papers published in AAIM'2021 and COCOA'2021 were selected among those of high quality and invited to their *special issues* in the journals *Theoretical Computer Science* and *International Journal of Foundations of Computer Science*, respectively.

Next, we present final remarks about our four innovative and pioneering projects.

Project 1. Although several works deal with complexity measures closely related to the notion of a succinct certificate, most of the literature results focus on discovering lower and upper bounds for these measures and characterizing related complexity classes. In this chapter, we address another direction, we introduce the SUCCINCT MONOTONE CIRCUIT CERTIFICATION problem and investigate its time complexity.

Project 2. The energy complexity measure represents an interesting manner to analyse the activation of gates through a circuit. Previous works address energy complexity in threshold circuits as a model that simulates a neural network. In this chapter, we introduce the discussion of energy complexity problems in terms of time complexity, and investigate the complexity to computing the best-case energy complexity of monotone circuits.

Project 3. To understand and identify potential gaps in the W-hierarchy, in this work, we proposed, using threshold circuits, a novel family of complexity classes of parameterized problems that are candidates for not being precisely covered in the W-hierarchy.

Project 4. Although the First and Best Improvement strategies have been widely studied on literature, little work has been devoted to exact move composition. This work presents a formal model of the MAXIMUM MULTI IMPROVEMENT PROBLEM, which gives the optimal combination of moves in a Multi Improvement neighborhood exploration.

7. Conclusion

During the doctorate process, many possibilities emerged from each seminar, class, or lecture. Since the beginning of this thesis writing, one idea has been clear: To avoid trivialities. With this purpose, our four projects detailed in previous sections aimed at the proposition of unexplored concepts. The problems SUCCINCT MONOTONE CIRCUIT CERTIFICATION, BEST-CASE ENERGY COMPLEXITY and MAXIMUM MULTI IMPROVEMENT are unprecedented (likewise the concept of Th-hierarchy). It is always risky to describe novel problems, measures, and concepts. It is impossible to predict the reception of the scientific community when it is faced with non-addressed problems. However, all concerns about the novelty of our projects were outdated. Besides, all those works receive positive answers from relevant international journals and conferences.

Referências

Dinesh, K., Otiv, S., and Sarma, J. (2020). New bounds for energy complexity of boolean functions. *Theoretical Computer Science*.

Downey, R. G. and Fellows, M. R. (2012). *Parameterized complexity*. Springer Science & Business Media.

Kanj, I., Thilikos, D. M., and Xia, G. (2017). On the parameterized complexity of monotone and antimonotone weighted circuit satisfiability. *Information and Computation*, 257:139–156.

Lennie, P. (2003). The cost of cortical computation. *Current biology*, 13(6):493–497.

Paterson, M. S. (1990). Improved sorting networks with o (log n) depth. *Algorithmica*, 5(1):75–92.

Robertson, N. and Seymour, P. D. (1984). Graph minors. III. Planar tree-width. *Journal of Combinatorial Theory, Series B*, 36(1):49–64.

Silva, J. C. N. (2021). *Algorithmic Aspects of Problems Related to Optimization, Circuits, and Parameterized Complexity*. PhD thesis, Universidade Federal Fluminense, Niterói, RJ.

Uchizawa, K., Douglas, R., and Maass, W. (2006). On the computational power of threshold circuits with sparse activity. *Neural Computation*, 18(12):2994–3008.