Electromigration Aware Cell Design

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Abstract. *Electromigration (EM) in on-chip metal interconnects is a critical reliability failure mechanism in nanometer-scale technologies. This work addresses the problem of EM on signal interconnects and on Vdd and Vss rails within a standard cell. An approach for modeling and efficient characterization of cell-internal EM is developed, incorporating Joule heating effects. We also present a graph-based algorithm that computes the currents when the pin position is moved avoiding a new characterization for each pin position and consequently reducing considerable the characterization time. We use the cell lifetime analysis to determine the lifetime of large benchmark circuits, and show that these circuit lifetimes can be improved up to 80.95% by avoiding the critical output, Vdd, and Vss pin positions of the cells, using minor layout modifications.*

1. Introduction

Electromigration (EM) is a major source of failure in on-chip wires and vias, and is becoming a progressively increasing concern as feature sizes shrink [Lienig 2013]. EM is initiated by current flow through metal wires and may cause open-circuit failures over time in copper interconnects. As consequence, circuits can stop work or work incorrectly, producing undesired results. Therefore, reduce the EM effects and increase the circuit lifetime is becaming a great and important challenge. We do not expect acquire an electronic product that will live just for a couple of months.

Traditionally, EM has been a significant concern in global power delivery networks, which largely experience unidirectional current flow. Recently, two new issues have emerged. First, EM analysis can no longer be restricted just to global wires. Traditional EM analysis has focused on higher metal layers, but with shrinking wire dimensions and increasing currents, the current densities in lower metal layers are also now in the range where EM effects are manifested. EM effects are visible at current densities of about $1MA/cm^2$, and such current densities are seen in the internal metal wires of standard cells, resulting in cell-internal signal EM [Jain and Jain 2012]. These high current densities arise because local interconnect wires within standard cells typically use low wire widths to ensure compact cell layouts. In short metal wires, such effects were traditionally thought to be offset by Blech length considerations, but such effects do not help protect intra-cell wires in designs at deeply scaled technology nodes. Second, EM has become increasingly important in signal wires, where the direction of current flow is bidirectional. This is due to increased current densities, whose impact on EM is amplified by Joule heating effects [Lee 2012], since EM depends exponentially on temperature.

Therefore, the current that flows through these wires to charge/discharge the output load can be large enough to create significant EM effects over the lifetime of the chip.

Intra-cell power networks are also associated with EM concerns. In going down to deeply scaled technology nodes, the current through the power rails of the cells has remained roughly constant while the cross-sectional area of power rails has decreased, causing the current density in power rails to increase [Wang et al. 2014]. Moreover, the power rails are generally subjected to a unidirectional current flow, referred as DC electromigration, which acts more aggressively in causing electromigration.

In the cell library used in this work, we can see high current densities on the Vdd and Vss power rails as well as on signal wires, reducing the lifetime of the cells. For example, we compute signal wires in an INV_X4 cell to have an effective average current density of 1.8 MA/cm^2 at 2GHz, while power wires have an effective current density of 2.15 MA/cm^2 in a 22nm technology. This switching rate is very realistic, and can be seen in, for example, clock buffers in almost any modern design.

While the cell-internal signal EM problem has been described in industry publications such as [Jain and Jain 2012], its efficient analysis is an open problem. The solution presented in this work is the first to analyze the EM effects inside of the logical cells in a circuit. Due to innovation and importance of this solution it has a patent application [Sapatnekar et al. 2015]. Moreover, the novelty and importance of this work can also be seen in a journal publication [Posser et al. 2016] and important conferences in the field [Posser et al. 2014a], [Posser et al. 2014b], [Posser et al. 2015c], [Posser et al. 2015a] and also a best paper in a regional conference [Posser et al. 2015b].

In this work, we study the problem of systematically analyzing cell-internal signal EM due to both AC EM on signal wires and DC EM on the Vdd and Vss rails of the cells. We devise a solution that facilitates the analysis and optimization of cell-internal signal EM for a standard cell library based design. We first develop an approach to efficiently characterize cell-internal EM over all output, Vdd, and Vss pin locations within a cell, incorporating Joule heating effects into our analysis. EM is modeled using the well-known Black's equation [Black 1969]. We then formulate the pin optimization problem that chooses cell output pins during place-and-route so as to maximize the lifetime of large benchmark circuits.

2. Problem Motivation

We motivate the problem using the INV_X4 (inverter with size 4) cell, shown in Fig. 1(a), from the 45nm NANGATE library [nan]. The input signal A is connected to the polysilicon structure. The layout uses four parallel transistors for the pull-up (poly over p-diffusion, upper half of the figure) and four for the pull-down (poly over n-diffusion, lower half of the figure), and the output signal can be tapped along the H-shaped metal net in the center of the cell. are numbered 1 through 7, and the edges of the structure are labeled e_1 through e_6, as shown in the figure. Since the four PMOS transistors are all identical, by symmetry, the currents injected at nodes 1 and 5 are equal; similarly, the NMOS-injected currents at nodes 3 and 7 are equal [Posser et al. 2016].

Let us first consider cell-internal signal EM. When the output pin is at node 4, the charge/discharge current is as shown in Fig. 1(b). Moving the pin changes the current

distribution in e_1–e_6. If the pin is at node 3 (Fig. 1(c)), since the rise and fall discharge currents have similar values, the charging current in edge e_2 is about $2\times$ larger than the earlier case, while the discharging current is about the same (with opposite direction). The larger peak current leads to a stronger net electron wind that causes EM, resulting in a larger *effective average current*, and therefore, a lower lifetime. Based on exact parasitic extraction of the layout, fed to SPICE (thus including short-circuit and leakage currents), the average effective EM current through e_2 is $1.17\times$ larger than when the pin is at node 4. Accounting for Joule heating, this results in a 19% lifetime reduction. For the Vdd and Vss pins, a similar effect occurs when the pin position changes.

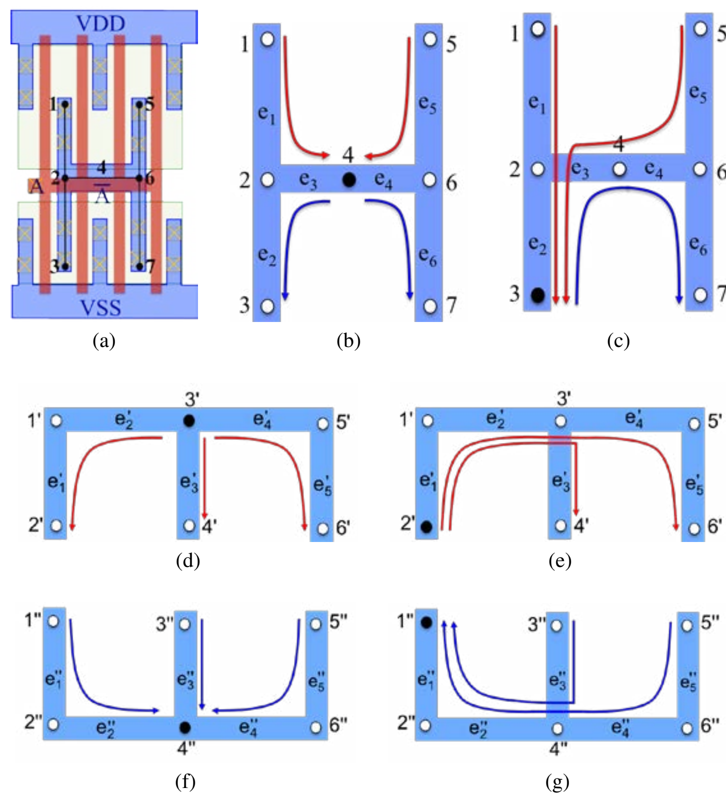

Figure 1. (a) The layout and output pin position options for INV_X4. Charge/discharge currents when the output pin is at (b) node 4 and (c) node 3. The red [blue] lines represent rise [fall] currents. (d) The Vdd pin position options for INV_X4 and the currents when the Vdd pin is at node $3'$ and (e) node $2'$. (f) The Vss pin position options for INV_X4 and the currents when the Vss pin is at node $4''$ and (g) node $1''$.

Next, we consider EM on the supply wires. Fig. 1(d) and (e) represent the Vdd rail, where the Vdd pin can be placed on the nodes numbered $1'$ through $6'$. Fig. 1(d) shows how the charge current is flowing through the edges when the Vdd pin is placed at node $3'$. We can see that the current flows are symmetric for this pin position. Since the edge e'_3 supplies two transistors, as shown in Fig. 1(a), the current flowing through e'_3 is larger than the current flowing through the other edges, which each supply just one transistor. Thus, the edge e'_3 is the critical edge when the Vdd pin is placed at node $3'$. Fig. 1(e) shows the current flowing through the edges when the Vdd pin is placed at node $2'$. In this case, the current flowing through edge e'_1 supplies three of the four transistors, is $3\times$ larger than the current flowing through this same edge when the pin is at node $3'$.

Thus, this is the critical edge for this pin position, reducing the lifetime of the cell by $2\times$ compared with the lifetime when the pin is placed at node $3'$. Similarly, the Vss rail of the INV_X4 cell is represented in Figs. 1(f) and (g). The Vss pin can be placed on the numbered nodes $1''$ through $6''$, and the currents being discharged through the edges by the Vss pin placed at node $4''$ are shown in Fig. 1(f). Using a similar argument as for the Vdd case, moving the pin from node $4''$ in Fig. 1(f) to pin $1''$ in Fig. 1(g) changes the critical edge from e''_3 to e''_1, and the lifetime again degrades by about $2\times$.

3. Current Calculation

The evaluation of EM TTF (time to failure) requires a characterization of (a) the average and RMS currents through a Vdd/Vss line and (b) the average currents, I^r_{avg} and I^f_{avg} and the RMS current I_{rms}. All of these parameters are both dependent on the pin position, as demonstrated in Fig. 1, and an obvious approach would be to enumerate the characterization over all possible combinations. Thereby, we develop a graph-based method for determining this redirection, and an algebra for computing I_{avg} and I_{rms} for each pin position based on the values from the reference case. Thereby, we developed an efficient graph-based algorithm to speed up the characterization of cell-internal over all output, Vdd, and Vss pin locations within a cell. This algorithm estimates the currents when the pin position is moved from a reference pin position to other one. In this way, a new characterization for each pin position is avoided, reducing the characterization time. Our algorithm produces an average error of just 0.53% compared to SPICE simulation.

4. Results

A method for optimizing the output, Vdd and Vss pin placement of the cells and consequently to optimize the circuit lifetime using minor layout modifications is proposed, just restricting the pin positions to the ones that reduces EM effects. Table 1 presents the results for a set of ITC'99 and ISCAS'89 benchmarks circuits mapped to our set of characterized cells and placed-and-routed. The results for Vdd and Vss pin placement are suppressed because the page limit, they can be seen in the Ph.D. dissertation. . For each benchmark the number of combinational cells, the clock period, total power consumption (leakage and switching power), area of core and total wirelength (WL) are presented, as reported by Encounter. These results correspond to a post place-and-route layout with no EM awareness, and the gap between the best and worst TTF values indicates how much the lifetime can be improved. The number of critical nets corresponds to the nets that violate the Joule heating constraint, and the number of critical cells corresponds to the cells that have pin positions that correspond to lifetimes below the best TTF. Interestingly, these numbers are both small, implying that large improvements to the lifetime can be obtained through a few small changes to the layout. Note that the best TTF values are in the range required for many modern applications (e.g., mobile devices) with short TTF specs of $3-4$ years. The lifetime of a circuit can be improved by up to 62.50% by altering the pin position of a few cells.

We now redo the routing step to guarantee that the best TTF in Table 1 can be met by outlawing all pin positions whose TTF is worse than the best TTF or with a Joule heating violation. Since the best TTF was computed by choosing the best pin position for each cell the circuit lifetime will be significantly enhanced. (Note that by the definition of best TTF, each cell is guaranteed to have at least one allowable pin).

Table 1. Cell-internal EM analysis for a set of benchmark circuits.

Circuit	# of comb. cells	Period (ns)	Power (mW)	Area of core (μm^2)	Total wire length (μm)	Worst TTF (years)	Best TTF (years)	TTF Improv.	# of crit. nets	# of crit. cells
b05	859	0.544	0.551	504	2682.50	4.07	6.53	37.59%	-	4
b07	461	0.306	0.352	317	1426.87	3.81	5.25	27.43%	-	3
b11	821	0.384	0.460	471	2439.83	2.75	5.82	52.80%	1	5
b12	1217	0.282	0.810	824	4236.15	3.13	3.14	0.15%	3	1
b13	340	0.208	0.467	272	1272.99	3.89	6.05	35.70%	1	7
s5378	1219	0.299	0.679	890	6418.27	2.74	3.59	23.67%	2	1
s9234	1044	0.373	0.584	849	4873.30	2.73	3.48	21.39%	-	1
s13207	1401	0.720	1.063	1733	7146.48	4.94	13.18	62.50%	-	7
s38417	10068	0.493	8.836	7959	46419.93	3.43	5.77	40.51%	2	6

After these new constraints are imposed on the pin positions, the router makes incremental changes to some interconnect routes. Table 2 shows the results after physical synthesis considering the best pin positions, i.e., for each cell, we disallow EM-unsafe pin positions. Thus, we see that the circuit lifetime is improved up to 62.50% while keeping the delay, area and power of the circuit unchanged, and with marginal changes ($\leq 0.15\%$) to the total wirelength.

Table 2. Performance impact of EM-aware physical synthesis using pin optimization.

Circuit	Period (ns)	Δ Period (%)	Power (mW)	Area (μm^2)	WL (μm)	Δ WL (%)
b05	0.544	-	0.551	504	2682.6	0.00
b07	0.306	-	0.353	317	1428.5	0.12
b11	0.384	-	0.460	471	2443.5	0.15
b12	0.280	-0.89	0.808	824	4112.8	-2.91
b13	0.208	-	0.467	272	1273.5	0.04
s5378	0.299	-	0.679	890	6422.2	0.06
s9234	0.373	-	0.584	849	4873.4	0.00
s13207	0.720	-	1.063	1733	7146.6	0.02
s38417	0.493	-	8.836	7959	46420.2	0.00

Runtime: As previously cited, the circuit analysis is executed by Encounter tool and the runtime for each benchmark is less than 40s. The critical pin positions for each circuit are reported in under 1s.

5. Conclusion

To our best knowledge, this is the first work that address the EM by optimizing the output, Vdd and Vss pin positions in cells improving the circuit lifetime. To optimize the TTF of the circuits just the LEF file of the critical instances is changed to avoid the critical pin positions. The cell layout is not changed. The circuit lifetime could be improved up to 62.50% at the same area, delay, and power. This is because changing the pin positions affects very marginally the routing. This lifetime improvement is achieved just avoiding the critical output pin positions of the cells [Posser et al. 2016], [Posser et al. 2014a], [Sapatnekar et al. 2015].

A lifetime improvement of 78.54% is achieved avoiding the critical Vdd pin positions and 89.89% avoiding the critical Vss pin positions. When the output, Vdd, and Vss pin positions are all optimized simultaneously, the TTF of the circuit could be improved up to 80.95% (from 1 year to 5.25 years). Considering the largest and smallest

lifetimes over all pin candidates for a set of cells, a lifetime of a cell can be improved up to 76$\times$ by the output pin placement. Some cells present a small TTF improvement when the output pin position changes, because the current densities through the edges are almost unchanged when the pin position changes. For these cells, layout optimizations are suggested to improve their lifetime [Posser et al. 2015a]. At circuit level, we present an analysis of the EM effects on different metal layers and different wire lengths for signal wires (nets) that connect cells [Posser et al. 2014b].

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