Neural Discriminating Analysis for a Nonintrusive Electrical Load Monitoring System

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Abstract

A nonintrusive electrical load monitoring system for household appliances is developed using neural networks. Appliances are characterized by features extracted from their transient and steady-state responses obtained from sampling information from the AC power line. A discriminating analysis is applied as an efficient way to achieve a compact neural discriminator which identifies seven classes of equipment. Over 100 different pieces of equipment studied, the system classifies correctly more than 90% of the sample. The system is implemented on a 16 node transputer based parallel machine to support massive application. A processing time smaller than 2 μs is achieved for each pattern.

1 Introduction

In Brazil, domestic power consumption responds for about one quarter of the total demand. Moreover, due to the new scenario established by global economy trends, this segment shows a continuous increase in its power demands. New products are continuously being introduced in the market, which represent new loads to the electrical system, and changes in federal policies can have a significant impact in this segment. As an example, a rise in air conditioning and refrigerating product demand was observed during 1995 due to import restriction decrease.

Thus, the knowledge of the power consumption profile of such segment can be considered quite relevant in terms of energetic planning. Domestic load monitoring can play a role in alleviating the electrical system in peaking periods, avoiding interruptions and delaying the needs of huge investments.

This work aims at developing a neural nonintrusive electrical load monitoring system for household appliances and implement it in a parallel machine. The design

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strategy comprises a preprocessing method for data compression and a discriminating analysis for achieving a compact neural discriminator. The implementation involves C code development for a 16 node parallel system. The parallel machine is based on a combination of fast digital signal processors (DSPs) and T9000 transputers.

In the next section, the monitoring system is described in details, including the preprocessing method, the achievements of the discriminating analysis, and system implementation. Results in terms of discrimination efficiency and processing speed are also presented in this section. Section 3 addresses conclusions.

2 The Load Monitoring System

The data used in this work concern measurements from the AC power line performed on different equipments, which were grouped into the following classes: refrigerating, resistive heating, universal motor, ventilating, consume electronics, incandescent lamp and fluorescent lamp. These classes are responsible for more than 95% of the total domestic electricity demand.

Appliances were characterized by their transient and steady-state responses. Transient analysis involved data acquisition with a digital storage oscilloscope with a sampling rate of 500 Sa/s, so that third harmonic information could be preserved. Starting from the time each appliance had been switched on and for roughly 2 seconds, current signals were acquired from the AC line and formed data words of 1024 samples. For the steady-state response, active and reactive powers and steady-state voltage were measured from a power transducer and a digital voltmeter after a minimum of 2 second working period. From these measurements, apparent current and phase angle were obtained. Figure 1 shows the block diagram of data acquisition system.

2.1 Preprocessing

Aiming at reducing the dimension of data input space, a preprocessing method based on envelope feature extraction and variance analysis was applied in the transient response [1].

The signal envelope is defined by the 60 Hz fundamental frequency of the AC line and shape features can be extracted by retaining the current peaks. From the original 1024 samples, 200 peaks were extracted. For this, a sliding window was used for detecting the maximum value in the set of samples that fall in between two neighbour zero crossing samples. Pre-trigger samples were neglected in this analysis.

The variance analysis was performed on the resulting vectors obtained from signal envelope analysis. Firstly, the mean value of the last 20 samples was subtracted from each vector, so that steady-state information could be eliminated from the transient signal. Next, the variance of each sample was computed. It was observed that the first 50 samples (417 ms) account for 95% of the normalized cumulative variance

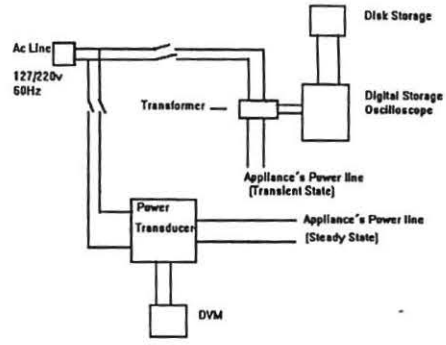

Figure 1: Data acquisition system.

sum. Therefore, the acquisition time window could be reduced by a factor of 4 by retaining only these more relevant samples.

In order to further reduce the dimension of data input vector, a spectrum analysis was applied. The Fast Fourier Transform was computed for each signal and most of the valuable information was observed to be restricted to 10 Hz for all classes but two which extended the relevant information up to 30 Hz. Based on Nyquist theorem, this implies that a 60 Hz sampling frequency would be enough for envelope representation. On the other hand, further analysis pointed out that this sampling rate needed to be maintained only for the first 10 samples, so that a 20 Hz sampling frequency was used for the remaining samples.

As a summary of the overall preprocessing method, from the original samples of signal envelope, ten samples were retained with a 16.7 ms period and five samples followed with 50 ms period until the last sample is reached. Including the two components derived from the steady-state analysis, raw data was translated into eighteen component data vectors, which were fed into the input nodes of the neural classifier. Typical preprocessed signals can be seen in Figure 2.

As the maximum starting current for all appliances was expected to be 100 A, this value was used as a fixed normalizing factor for all samples of the transient signal. Similarly, the steady-state current was normalized by a fixed 50 A current. This fixed normalization is valuable in terms of system implementation, as the normalizing factor can be stored in processor memories and extra processing is not necessary to perform sample normalization.

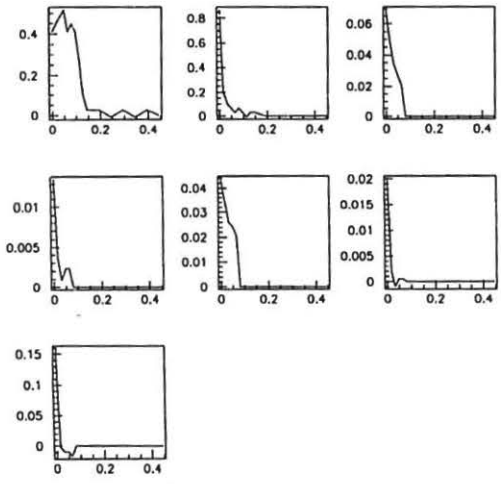

Figure 2: Typical transient signals from each of the seven classes after the preprocessing method is applied. Time is in seconds.

2.2 Discriminating Analysis

The discriminating analysis aims at finding a reduced number of directions in the input data space able to efficiently discriminate events from different classes.

In order to have a compact neural network to perform the classification task, principal discriminating components were extracted from preprocessed data. The neural discrimination was then performed by projecting the preprocessed data vector into these discriminating directions, which are found at the input layer of the neural network.

Figure 3 shows how the principal discriminating components were extracted. The backpropagation training procedure [2] was used for a scalable network built by increasing the number of discriminating components up to the point where the discrimination efficiency could not increase for the overall seven classes that were to be identified. For this single hidden layer neural network, each time a new component was added, in the form of adding a new neuron in the hidden layer, the hidden layer of the network was trained just for the weights which connected the input nodes to this new added neuron. The other weights in this layer remained frozen, as they represented discriminating components already extracted. The weight vectors that connected the hidden layer to the output layer were retrained for each new component added, so that the network could search for the best way to combine the contribution of each component of the new set of discriminating components.

The neural networks used along this paper were simulated by means of JETNET

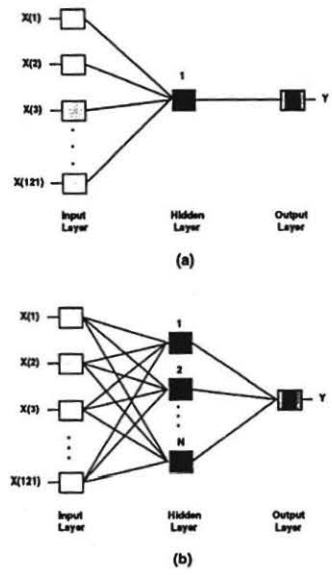

Figure 3: Principal discriminating component extraction: first (a) and N-th (b) components are shown. For simplicity, the output layer is represented by a single neuron.

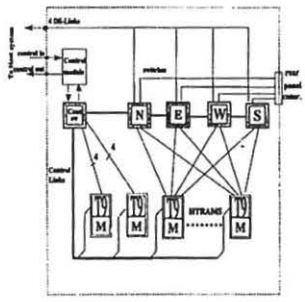

Figure 4: The basic architecture of TN 310 system. Extracted from [5].

2.0 package [3]. The selected activation function for the neurons was the hyperbolic tangent. The fully-connected feedforward networks comprised seven neurons in the output layer and each one of these neurons was assigned to a given class, so that maximum probability was used to detect the winning class for a given pattern presented at the input nodes of the network. The target vector for the training phase was defined by establishing a target value of 1 to the output neuron that represented the class to which belongs the pattern being presented to the network and filling the rest of the vector's components with -1. The sample space included 100 different pieces of equipments and half of this was used for training and the other half was only involved with testing.

For comparison, a network was trained using backpropagation and disregarding the principal discriminating component analysis. For a network comprising 18 input nodes and seven nodes in the hidden layer, 84% of the sample was correctly classified. On the other hand, after extracting four principal components, more than 90% of the sample was correctly classified. It should be noticed that, as from Figure 3, the network in this case has only 4 nodes in the hidden layer, which means that the number of multiplications involved in processing a given pattern is reduced almost by a factor of two, when the two neural networks are compared. Thus, principal discriminating component analysis can provide a more compact and faster discriminating system.

It should also be mentioned that the classifier is working based on a reduced statistical sample and possible improvements in performance can be achieved if a larger set of data can be recorded and used in the network's training phase.

2.3 System Implementation

The implementation of the load monitoring system considered two aspects. In the

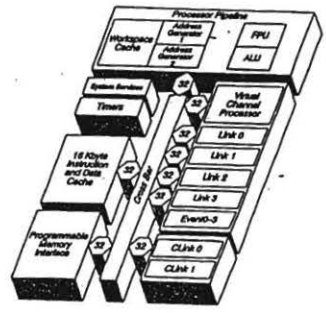

Figure 5: T9000 transputer. Extracted from [5].

first, the flexibility of technology was addressed and digital signal processors (DSPs) were considered as a feasible solution. DSPs can accommodate a different number of applications and support high-level language programming, like C, in different platforms. Moreover, neural processing is very suitable to be implemented in this technology, as the main computation required by this technique is inner products which, in fact, represent one of the main concerns in DSP designs. Also, demanding processing speed requirements can be met by fast DSPs currently available in the market at a reasonable price. A classifier based on principal discriminating analysis was previously implemented in such technology with quite good performance [4]

The second aspect addressed processing parallelism. As neural processing exhibits a natural parallelism, ultimate speed can be achieved by exploring this feature. Here, communication among processes can be thought to be efficiently realized by using transputers.

Combining both aspects, the TN-310 system (see Figure 4) was selected for system implementation. This is a 16 node transputer based parallel machine that uses fast DSPs (ADSP-21020) running as coprocessors to the transputers (T9000). Thus, the architecture of such system tries to combine the T9000 capabilities for process communication and the optimized signal processing implementation by means of the DSP.

The TN 310 system is a multiple instructions multiple data parallel computer with a distributed memory architecture [5]. This means that each node has its own local memory. The system in consideration houses 16 nodes based on T9000 transputers, which communicate with each other by means of a network of C104 chips. Each node has access to the communication network through four high speed (100 Mbits/s) serial links (DS-links), which allow it to access data held anywhere in the system.

The T9000 transputer is a 32-bit microprocessor that allows multiple instructions to be executed at every processor cycle. Figure 5 shows the T9000's architecture. It supports the creation and scheduling of any number of concurrent processes. For inter-process communication, the instruction set includes specific instructions. Thus, communication between processes running on a single transputer or running on separate transputers is possible.

Communication between processes takes place over channels, and is implemented in hardware. Communication between processes on different processors takes place over virtual channels. Multiple virtual channels are multiplexed onto each physical link by the virtual channel processor. With virtual channels, it is not necessary for the programmer to allocate channels to physical links, and the allocation of processes to processors is simple.

The C104 is able to connect 32 high bandwidth serial communication links to each other via a 32 by 32 non-blocking crossbar switch, enabling messages to be routed from any of its links to any other link. The TN-310 system uses four C104s, each one connected to a corresponding link of the T9000s.

All nodes of this machine complies to the Standard HTRAM (High performance TRAnsputer Modules) specification, which allow to use a fast DSP for signal processing applications. 256 kbytes SRAM is used as shared memory, to transfer data to and from the DSP coprocessor. The DSP HTRAM also includes 8 Mbytes of T9000 private DRAM. The ADSP 21020 can be programmed from the T9000 through C runtime library calls.

The 32-bit floating point DSP used (ADSP-21020) [6] runs at 25 MHz clock speed. The basic architecture (see Figure 6) of this device includes three independent computational units: ALU, multiplier with fixed-point accumulator and shifter. The units are connected in parallel and can use up to 16 internal registers at any moment. Every instruction is executed in a single cycle, which implies that multiplication with accumulation and search for the next operands can be performed in one cycle.

The TN 310 system can be accessed through a host machine, in our case a PC running MS-DOS and Windows. Applications can be developed using a C toolset layer of programming that provides ultimate processing speed.

The load monitoring system was implemented in the TN-310 system including both data preprocessing and neural processing. For each pattern to be identified, the data fed into the system comprised the 200 sample vector from signal envelope. The neural network's weights obtained from principal component analysis and the normalizing factors were stored in memory.

The parallelism of actions was based on one processor acting as a manager of the overall system, whilst the other 15 processors were allocated for neural processing [7]. The managing processor was continuously feeding data to the other processor and was the only processor to communicate with the host. Therefore, all input and output information passed through this processor. Using such approach, the processing time for a pattern was measured to be in average smaller than 2 μs.

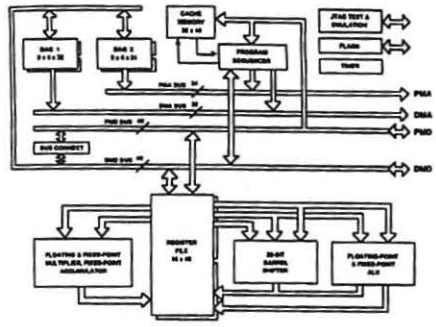

Figure 6: The basic architecture of ADSP-21020. Extracted from [6].

3 Conclusions

A nonintrusive system for electrical load monitoring has been presented. It was based on acquiring data from the AC power line concerning steady-state and transient analysis. Data compression was obtained by a combination of signal envelope feature extraction and variance analysis supported by a spectrum analysis. The system used neural networks to classify pieces of equipment from seven different classes. The neural network was designed by using principal discriminating component analysis, so that a compact and high-efficiency classifier could be achieved. Over a total sample of 100 pieces of equipment, the system using four components (a 18-4-7 network) classified more than 90% correctly. Besides being quite compact, this approach improves the original performance of a 18-7-7 network trained without principal component considerations.

The compact load monitoring system was implemented in a transputer-DSP based parallel machine housing 16 processing nodes. The application was described in a *C* toolset environment and processes were coded in *C* language. Less than 2 μs were required to process in average each pattern in such system.

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