Dealing with the Obsolescence of Programmable Logic Devices (PLDs) in Electronic Products

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Abstract. *PLDs are commonplace in today's electronic products. When such devices reach their end-of-life, the product manufacturer must find a viable solution, both technical and economical. Replacing a PLD by an ASIC is a viable alternative that is explored in this paper, using a real case as an example. Boundary business conditions for deciding for this option are presented. Depending on these conditions, obsolescence can be seen as an opportunity for the improvement of the product, taking advantage of other benefits that an ASIC brings. As an ASIC development can be seen as risky, pricy, and as having a long time to market, a structured ASIC platform, called ICX, that mitigates all of these three aspects, is also presented.*

1. Introduction

Programmable Logic Devices (PLDs) are usually divided into three types: Programmable Logic Arrays (PALs), Complex PLDs (CPLDs), and Field Programmable Gate Arrays (FPGAs). The first two types of PLDs are commonly used in applications that require simple digital logic, while FPGAs are often used in more complex systems. All these devices, however, represent alternative solutions to off-the-shelf components. Another option for product development is to consider an Application Specific Integrated Circuit (ASIC). The choice among the possible solutions (PLDs x Off-the-shelf Parts x ASICs) for the implementation of an electronic product is based on many factors such as: final product cost, production volume, development time, development risk and performance constraints (high speed, low power, for instance).

The main advantage of PLDs is their capability to be re-configured [1]. This allows companies to change the product logic without modifying the printed-circuit board (PCB) in which it is used, as long as the PLD of choice is available. For this reason it is common that products are developed using PLDs and, unfortunately, every year many components (including PLDs) are discontinued or become obsolete due to product end-of-life (EOL). In this case, a product's PCB re-design could be avoided by converting the circuit from the PLD into a pin-to-pin compatible ASIC.

This paper describes two possible solutions for the replacement of obsolete components. The first solution is the direct conversion of the PLD into an ASIC using a package that is pin-to-pin compatible. The technical and business aspects of this option are discussed. The second option is the migration from PLD to a mixed-signal ASIC with improved functionalities. For such a migration, this article also describes the ICX

platform [2] which enables both replacement of the digital circuitry as well as the addition of analog peripherals.

2. Business aspects

It is widely known that the development of a product requires a large investment (both money and time) to obtain robust, user-friendly and fashionable designs. On top of mature hardware and software, several applications require qualifications which further add cost and development time. For this reason, changes in a proven and qualified product should be avoided as they will have a direct impact on the availability of the referred product to the market.

Given the constraints described above, after all the work, money and time invested in the development of a product, the end of life of a key electronic component can have huge impacts. Unfortunately, this kind of situation is frequent and a viable solution should be available when it happens.

The business decision of how to solve an obsolescence problem is not trivial. It will depend on the volume of the production, return of investment of NRE, schedule, application, among several others. Every case should be cautiously studied with each unique condition faced by individual companies.

Although the problem is not simple, replacing the EOL'ed part by a pin-to-pin compatible ASIC should always be considered a viable path as it allows the company to:

1. reuse the existing design (RTL, PCB, boxing, etc);
2. avoid expensive and time consuming requalifications;
3. gain control of the supply chain of key components;
4. reduce risk when compared with a new design cycle.

In order to keep the availability of the product during the design of the replacement part, it is advisable that the manufacturer builds inventory of the EOL'd device that will cover the development time [3]. This period varies from 9 months to 18 months in most cases.

Assuming that replacement of the part is chosen to be the most viable way, the phases described below should be covered.

1. Preliminary studies

It is important in this phase to understand if the replacement is technically feasible and to obtain estimates in terms of NRE, schedule, and unit price for the ASIC that will replace the part. The main goal at this moment is to have enough information to support the decision to be made. At this moment it is important to have key information such as expected production volume, expected replacement schedule, availability of inventory, specific needs for qualification and system level specifications.

2. Specification capture

Once a decision for the replacement is made, a careful study of the PLD and its application must be conducted, including the RTL codes so that a clear view of issues

such as number of gates, need for analog circuits (if applicable), memory (if applicable), IO voltages, and speed can be formed.

Having this information in hand, the confirmation of the foundry and technology node must be done, together with IP procurement (analog, PLL, memories, standard libraries, IO cells). These aspects should have been already considered in Phase 1, mainly because of cost issues.

3. Implementation

The technical activities that will take place in this phase will be mentioned in Section 2. The implementation flow of a digital ASIC with analog IP and memory has been widely discussed [4]. However, it is worth noting that in this phase the details of performance and desired behavior of the chip should be carefully considered.

4. Manufacturing

The manufacturing of a silicon wafer is also well covered in the literature [5] and each step of the manufacturing process has its own technical expertise and knowledge. Once the processed wafers are delivered by the foundry, a series of post-processing steps are performed towards the packaged chip. These steps include wafer backgrinding and dicing, packaging and tests.

The production tests are very important to sort out any sample that presents manufacturing defects.

5. Logistics and delivery

It is important to mention that the semiconductor supply chain is spread all over the world and it is very common to have the ASIC samples shipped from and to different locations for each step of the process. Hence, the importance of the logistics and the obtention of export control clearances cannot be neglected.

3. Direct PLD-to-ASIC Conversion

The process of converting a PLD circuit into a pin-to-pin compatible ASIC involves executing the ASIC design flow from an already available hardware description, usually in the form of Hardware Description Language (HDL) files. This already reduces the development time of the ASIC (and cost), leaving only the “backend” flow to be executed. This design flow comprises logic synthesis, floorplanning, power planning, logic synthesis, placement, clock tree synthesis, routing and final physical checks, mainly Design Rule Check (DRC) and Layout-Vs-Schematic (LVS).

After executing the ASIC design flow, the design is taped out, followed by the wafer fabrication, wafer post-processing (backgrinding and dicing), packaging and testing. Package requirements as well as electrical and functional parameters must be guaranteed by the ASIC vendor.

Part of the activities mentioned above represent a non-recurring-engineering (NRE) cost. These are: the ASIC design, the wafer fabrication masks, the package tooling, the production test development and the qualification tests. The final ASIC unit cost is calculated considering the following costs: wafer fabrication, wafer backgrinding and dicing, packaging and production test execution. The unit cost of the final chip will

very often be lower than the PLD being replaced although this cost is highly dependent on the production volume. Also, it is possible to achieve better performance in terms of power consumption when comparing with the original PLD.

3.1 Case study : CPLD to ASIC conversion

One success case is the replacement of the Intel/Altera MAX7064ATC44-10 CPLD [6] by an ASIC. The motivation for this replacement was due to part obsolescence: the PLD that was used in the product was an old CPLD that reached End-of-Life [7]. The replacement of the referred CPLD for an updated one could be a possible solution, however, this would cause changes in the product that the manufacturer was not willing to make, such as changes in the bill of materials (BOM), redesign of PCB, eventual requalification of product, among others.

As a rule of thumb, production volume of around 10,000 units/year associated with a product life expectancy of at least another 5 years could lead to a feasible business solution using the conversion of the logic in the CPLD to an ASIC, as final part price would be comparable to old CPLD price and no adjustment would be necessary to the product manufacturing process.

The design implemented in the original CPLD was composed of a simple logic and some SRAM memory blocks (CPLD built-in memories). The same HDL files that were used by the CPLD to implement the logic were used as input to the design flow of the ASIC, thus bypassing the costly RTL development and verification phase of ASIC design.

Target technology selection was done taking into account electrical and timing constraints as specified by the original CPLD (in order to keep parts compatible). These constraints allowed the selection of a conventional IC technology (0.35μm), thereby reducing the complexity and production costs associated with the ASIC development. All needed IP libraries (standard cells, IO cells and SRAM IP blocks) were also provided by the chosen silicon foundry.

During logic synthesis, the logic described in HDL files was mapped to standard cells and memories were mapped to SRAM IP blocks. In this step, the only structures that were new compared to the design that was used in the original CPLD were the IO cells. These cells needed to be added according to the specification from IO assignment in the original CPLD.

The floorplan was done by placing the mapped netlist into the chip core area which is surrounded by IO cells. After defining chip floorplan and power plan, cells were placed and routed and design was verified (complete physical verification).

After design was concluded and the ASIC was fabricated, it was packaged according to the specifications of the part being replaced (original CPLD used a 44-pin package of the PLCC type), following the same exact pin order to guarantee PCB footprint compatibility between the ICs. The ASIC was then tested and was ready for volume production. Figure 1 shows a photograph of the packaged ASIC in its test fixture.

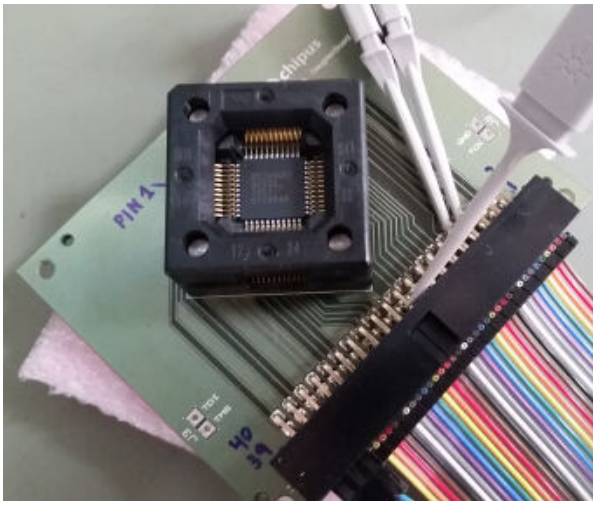

Figure 1. ASIC under test

The total development cycle, from starting the logic synthesis based on the original CPLD HDL files until the first production lot being fabricated, was around 10 months. Side benefits from this part replacement included lower power consumption and total control over the supply chain of the ASIC.

4. Migration from PLD to ASIC with improved features

When a PLD comes to obsolescence it can also be an opportunity to improve the product in which the PLD is used. One way to achieve this is to migrate the PLD to an ASIC further integrating other functionalities. In this case, as the name suggests, an application-specific IC can be designed to include, beyond the PLD logic, features that improve the product's performance, cost and/or protection against counterfeit.

In this migration process, components can be removed from the board and integrated into the ASIC, thereby decreasing the BOM and, consequently, the final product cost. The reduction of cost brough by a reduction in the BOM is twofold: firstly, it means less components to be purchased and, secondly, it reduces the pick and place time in the PCB assembly process.

The opportunity of designing an IC customized for a given product also opens the possibility to optimize the product performance in terms of speed or power consumption, to name just a few options. Also, features that were not possible due to the inexistence of off-the-shelf components, could possibly be added. Last, but not least, when integrating more functions inside an ASIC, it becomes more difficult and more expensive for a product to be reverse engineered and copied.

It is true, tough, that designing an ASIC from scratch involves an important investment in NRE. The time for the ASIC development until it can be used in volume production must also be considered. The technical risk, meaning the risk that something does not work according to the specification, must also be taken into account and this is inherent to the IC design activity.

To address those three issues (cost, development time and risk) of an ASIC design, we have developed a platform based on the structured ASIC concept [2], explained in the next section.

4.1. The ICX Platform

The ICX platform [2] is a structured ASIC chip that combines the use of mask-configurable logic, a One-Time-Programmable (OTP) non-volatile memory (NVM), and analog circuits, such as A/D converters, D/A converters, LED drivers, load switches, power management circuits, and general-purpose operational amplifiers and comparators,. A photomicrograph of an ICX demonstrator chip is shown in Figure 2.

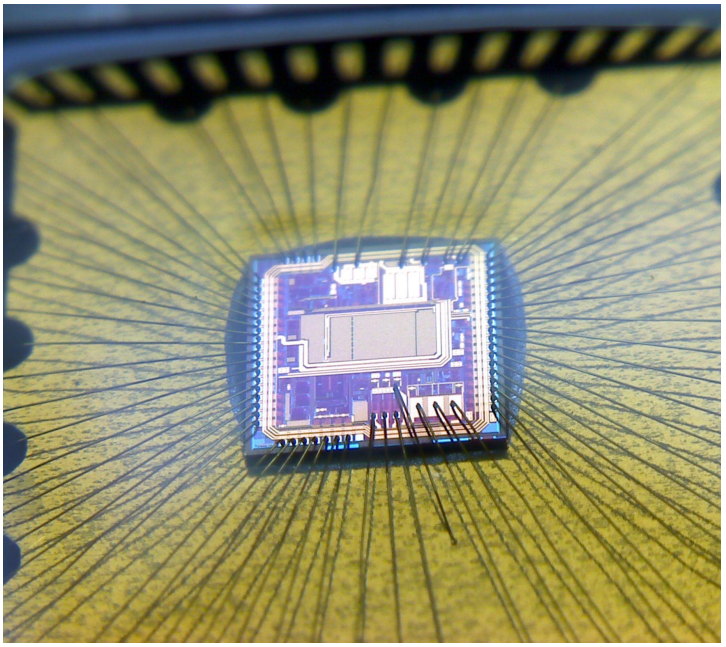

Figure 2. Micrograph of an ICX die mounted in a QFN64 package.

For the case of a PLD-to-ASIC migration, the mask configurable logic is used to implement the PLD logic. In the flowchart shown in Figure 3, the HDL from the PLD is the input for the logic synthesis and all previous steps can be eliminated. All the circuits contained in the ICX ASIC are ready for use and only need to be configured. Part of the configuration can be done after fabrication and saved on its NVM. The other part is mask-configurable, like the logic. Hence, in the fabrication flow, only the Back-End Of the Line (BEOL) masks (metals and vias) need to be customized.

The main advantages of using the ICX ASIC are i) the NRE cost reduction, since all circuits are silicon proven and part of the fabrication process is already done, ii) the reduction of risk associated with the design of analog circuitry given that all analog circuits were previously proven in silicon, and iii) reduction in development time inherent to the process of reusing RTL from PLD and proven analog circuits.

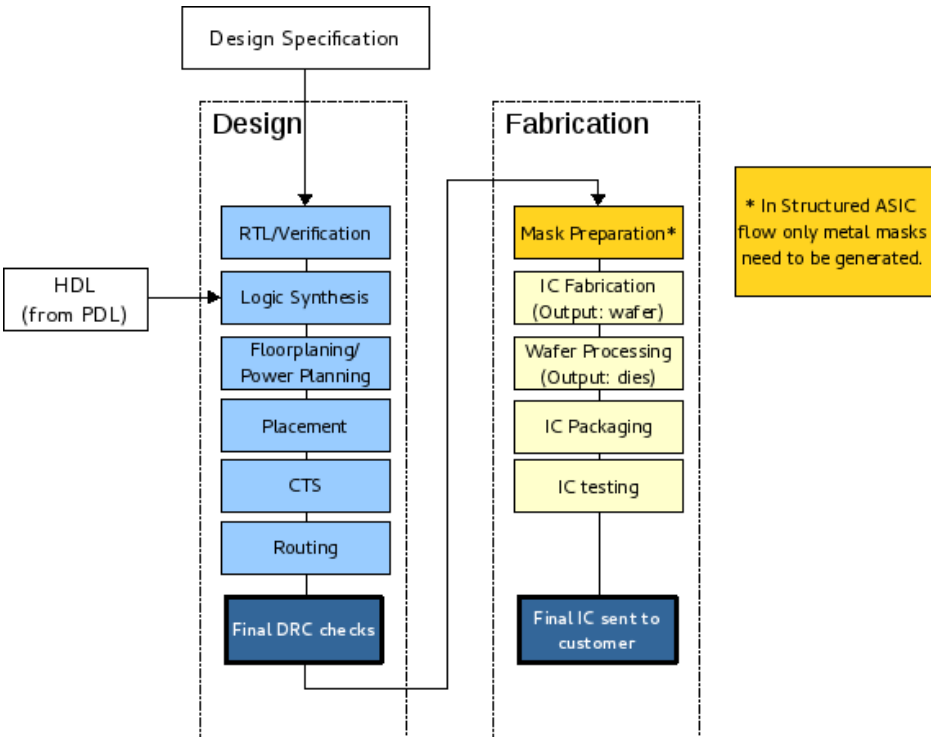

Figure 3. PLD-to-ASIC migration flowchart using the ICX Platform

5. Conclusion

As new PLD components become available, several components have become obsolete in a natural evolution process of the semiconductor industry. Companies with successful products that use obsolete components tend to adapt the solution when such an event happens. Replacing the obsolete components by an ASIC should be treated as a viable path to follow as it brings several benefits other than solving the obsolescence problem.

In this article we described some business aspects of this replacement when pin-to-pin compatibility is required and presented a success case of a PLD-to-ASIC conversion. The conversion was driven by the obsolescence of Intel/Altera MAX7064ATC44-10 and took 10 months.

In case the obsolescence is faced as an opportunity to improve the product that employs the EOL'ed component, the design of an ASIC brings further benefits. In this case, not only the obsolete part will be replaced but other features can also be added to the chip reducing the bill of materials, PCB area and time required for assembly by the pick-and-place machine. Chipus' ICX platform was briefly described as a possible manner to reduce ASIC development time, cost and risk.

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